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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fourth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Sep. / Oct. - 2023

Digital Design Using Verilog HDL

Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1: Apply the knowledge of digital fundamentals to explain basic concepts used in Verilog HDL.
CO2: Write a Verilog model for combinational and sequential circuits.
CO3: Analyse the given digital circuit and develop Verilog model for given digital circuits.
CO4: Design any combinational and sequential circuits and develop Verilog model for the given inputs.
CO5: Verify the design through synthesis and demonstrate the application using EDA tools.

***Note**: I) **PART - A** is compulsory. **Two** marks for each question.*

*II) **PART - B**: Answer any **Two** sub questions (from a, b, c) for a Maximum of **18 marks** from each unit.*

Q. No.	Questions	Marks	BLs	COs	POs
	I : PART - A	**10**			
1 a.	List any two differences between blocking and non-blocking statements in Verilog.	2	L3	CO1	PO1
b.	Difference between wire and reg in Verilog.	2	L2	CO2	PO2
c.	Differentiate between distributed delay and lumped delay.	2	L2	CO1	PO1
d.	Write Verilog description of 4:1 MUX using UDP.	2	L2	CO1	PO1
e.	Define temporal and static assertion checking.	2	L2	CO5	PO3
	II : PART - B	**90**			
	UNIT - I	**18**			
2 a.	Discuss lexical conventions used in Verilog HDL with syntax.	9	L2	CO3	PO2
b.	Explain the data types available in Verilog HDL with examples.	9	L2	CO1	PO1
c.	Develop a Verilog code for 4-bit ripple carry counter using data flow modeling.	9	L3	CO1	PO1
	UNIT - II	**18**	L2	CO2	PO1
3 a.	Discuss procedural blocking and non-blocking assignment with examples.	9	L2	CO1	PO1
b.	Explain delay based timing control with examples.	9	L2	CO3	PO2
c.	Develop syntax for the task declaration and invocation and explain with examples.	9	L3	CO1	PO1

Contd…2

	UNIT - III	**18**			
4 a.	Develop a Verilog code for 'D' flip flop using assign and de-assign continuous assignment statements (procedural).	9	L3	CO3	PO3
b.	Explain conditional compilation and execution with Verilog syntax.	9	L2	CO3	PO2
c.	Discuss types of delay models with Verilog syntax code	9	L2	CO4	PO3
	UNIT - IV	**18**			
5 a.	Develop a Verilog code for 4-bit synchronous up counts using UDP primitives.	9	L3	CO4	PO3
b.	Discuss PLI library routines and develop PLI routine for "get module post list" with syntax.	9	L2	CO4	PO3
c.	Draw and explain the flowchart for logic synthesis chart from RTL to gates.	9	L3	CO5	PO3
	UNIT - V	**18**			
6 a.	Explain formal and semi-formal verification.	9	L2	CO5	PO3
b.	Explain the flowchart for traditional verification of VLSI chip.	9	L2	CO5	PO3
c.	Discuss assertion checking using appropriate schematic block.	9	L2	CO5	PO3

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