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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Computer Science and Engineering

Semester End Examination; Dec. - 2014

Digital Logic Design

Time: 3 hrs *Max. Marks: 100*

***Note** : i) Answer **FIVE** full questions, selecting **ONE** full question from each Unit.*
ii) Assume suitably missing data if any.

Unit - I

1. a. What are universal gates? Realize the following functions using minimum No. of any universal gates. 8

   i) $a\bar{x} + \bar{a}x + axy.(\bar{a}+\bar{x}+\bar{y})$

   ii) $\overline{\bar{a}\bar{b}}+ab$

   b. Simplify the following functions using K – map.

   i) $F(a,b,c,d)=\sum m(1,2,8,9,13)+d(0,5,10)$ 6

   ii) $F(w,x,y,z)=\pi m(0,2,5,7,8,14)+d(4,6,10,12)$

   c. Simplify the following function using two variables K – map.

   $F(a,b,c)=\sum m(0,2,4,6,7)$ 6

   [Note : take 'C' inside the map) and realize using logic gates.

2 a. What is the advantage of Quine-Mc Clusky method over K map?

   Simplify the following function using Quine – Mc Clusky method. 10

   $F(a,b,c,d)=\sum m(3,6,7,11,12,13,14,15)$

   b. Design a 4 input 1 output logic circuit that outputs

   i) '1 when no. of '1's in the input is greater than no. of '0's. 10

   ii) '0' when no. of '1's is less than no. of '0's.

   iii) don't care other wise.

Unit - II

3 a. Design seven segments Decoder circuit. 10

   b. Design BCD to Excess-3 code converts circuit. 10

4 a. Implement full adder using 4 : 1 multiplexer. 6

   b. What is comparator? Design 2 bit comparator circuit. 8

   c. Design 2 bit fast adder. 6

Contd…2

Unit - III

5	a.	Explain J.K. master slave Flip-Flop.	7
	b.	Derive characteristic equations for SR, K and T flip flop.	9
	c.	How do you design the following, i) D Flip-flop using SR Flip Flop. ii) T Flip – Flop using JK Flip Flop.	4
6	a.	Explain the design of following shift registers: i) Serial in serial out. ii) Parallel in Parallel out.	10
	b.	Design sequence detector and sequence generator circuit using shift register.	10

Unit - IV

7	a.	Design a synchronous 3bit counter T-Flip Flop that has the following containing sequence 0, 2, 4, 6, 7, 0 .	10
	b.	Explain successive approximation A/D converter with a neat diagram.	10
8	a.	Design 3 bit asynchronous up counter using JK flip flops.	10
	b.	Explain Dual slope A/D converter circuit.	10

Unit - V

9	a.	Write VHDL Code for full adder and Full subtractor.	10
	b.	Briefly explain TTL parameters.	10
10	a.	Write VHDL code for 2 : 4 decoder and 4 : 1 multiplexer.	10
	b.	Explain CMOS NOT, NOR and NAND circuits. How CMOS differs from TTL?	10

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