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P.E.S. College of Engineering, Mandya - 571 401
(An Autonomous Institution affiliated to VTU, Belgaum)
Third Semester, B.E. - Computer Science and Engineering
Logic Design

Time: 3 hrs   *Max. Marks: 100*

Note: *Answer any **FIVE** full questions, selecting at least **TWO** full questions from **each part**.*

PART - A

1.a	What are universal gates? Realize basic gates using any one of the universal gate.	8
b.	Convert the given expression in standard SOP forms; $i) f(A,B,C) = A + AB + CB$ $ii) f(P,Q,R) = PQ + R + PR$	8
c.	Simplify the following Boolean equation using Boolean laws. $Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + AB\overline{C}$	4
2.a	Reduce the following function using K-map technique and implement using gates. $i) f(P,Q,R,S) = \sum m(0,1,4,8,9,10) + d(2,11)$ $ii) f(A,B,C,D) = \Pi M(0,2,4,10,11,14,15)$	10
b.	Simplify the following Boolean function by using QM method $F(A,B,C,D) = \sum m(0,2,3,6,7,8,10,12,13)$	10
3.a	Implement the following Boolean function using 8x1 MUX $F(A,B,C,D) = \sum m(0,1,2,4,6,9,12,14)$	10
b.	What is carry look ahead adder? Design 2-bit carry look ahead adder.	10
4.a	Give the characteristic equation, state diagram and excitation table of SR, JK and T flip flop	9
b.	Convert SR flip flop to JK flip flop	6
c.	Explain Master slave JK flip flop.	5

PART - B

5.a	Explain serial in serial out and parallel in serial out register with a neat Logic diagram	10
b.	Explain the working of Johnson counter and Ring counter	10
6.a	Design a synchronous mod-3 counter with the following sequence using clocked JK flip flops count sequence $\rightarrow$ 0, 1, 2, 0, 1, 2	10
b.	Draw and explain the working of 4 bit up/down synchronous counter.	10
7.a	Explain state reduction technique with a neat diagram.	10
b.	Distinguish between Mealy model and Moore model.	10
8.a	Explain dual slope A/D conversion with a neat diagram.	10
b.	Explain R-2R ladder D to A conversion.	10

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