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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Computer Science and Engineering

Semester End Examination; Dec. - 2015

Digital Logic Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each **unit**.*

UNIT - I

1 a. Realize $y = AB + \overline{C}$ using only NOR gate and write the truth table. 6

b. Simplify the following Boolean equation using K - map :

i) $F(A,B,C,D) = \sum m(1,2,3,6,8,9,10,12,13,14)$

ii) $F(A,B,C) = \left(\overline{A}+\overline{B}+\overline{C}\right)\left(\overline{A}+B+\overline{C}\right)\left(A+B+\overline{C}\right)$. 8

c. Simply the function using K – map,

F(a, b, c, d) = Σ m (2, 3, 4, 5, 13, 15) + d(8, 9, 10, 11),

Using 'd' as don't care term. Realize a AND - OR gate network using minimum number of gates. 6

2 a. Explain the principle of duality with example. 4

b. Get the simplified SOP expression of,

Y = F(w, x, y ,z) = Σ m (1, 2, 8, 9, 10, 12, 13,14)

Using Quine - McClusky method. 8

c. The input to a combinational circuit is a 4 bit binary number. Design the logic circuit with minimum gates for the following condition,

i) Output g_1 = 1, if the input binary number is 5 or less than 5

ii) Output g_2 = 1, if the input binary number is 9 or more than 9. 8

UNIT - II

3 a. Implement the following Boolean function using (i) 16:1 mux and ii) 8:1 mux

$F(P,Q,R,S) = \overline{P}Q\overline{S} + PRS + \overline{Q}RS + \overline{P}\overline{R}S$ 8

b. A combinational circuit is defined by the functions,

F_1 = Σ m (3, 5, 7) F_2 = m (4, 5, 7),

Implement the circuit with a PLA having 3 inputs, 3 product terms and 2 outputs. 4

c. Design BCD to EXCESS - 3 code converter. 8

4 a. What is fast adder? Design 2 bit fast adder using suitable equations. 6

b. Design an octal to binary encoder. 4

Contd…2

c. Implement the following Boolean function using PAL :

w(A, B, C, D) = Σm(0, 2, 6, 7, 8, 9, 12, 13)

x(A, B, C, D) = Σm(0, 2, 6, 7, 8, 9, 12, 13, 14) 10

y(A, B, C, D) = Σm(2, 3, 8, 9, 10, 12, 13)

z(A, B, C, D) = Σm(1, 3, 4, 6, 9, 12, 14).

UNIT - III

5 a. For JK and T flip flop give,

i) State transition diagram

ii) Characteristic equations 8

iii) Exitation table.

b. A Binary number 10111011 is serially shifted (right) into a eight bit parallel out shift register that has an initial content by 10101010

i) What are the Q outputs after 2 clock pulses 6

ii) After 4 clock pulses

iii) After 8 clock pulses.

c. Draw the circuit and explain the working of a 3 bit Johnson's counter. 6

6 a. Convert SR to JK flip flop. 8

b. What is race around condition? Explain how it is eliminated using JK master slave flip flop. 6

c. Explain with suitable circuits how shift register can be used as a sequence detector. 6

UNIT - IV

7 a. Design Mod - 6 synchronous up counter using JK flip flops. 10

b. Design a 2 bit down counter using D flip flop. 6

c. With a neat block diagram explain successive approximation technique. 4

8 a. Design a self correcting Mod - 6 counter in which all the unused states leads to state "000". 7

b. Design a counter to generate the following sequence using D flip flop,
0-3-5-4-2-6-1-7-0. 8

c. Explain dual slope A/D converter with a neat diagram. 5

UNIT - V

9 a. Write the VHDL code for the following :

i) 4:1 multiplexer ii)Johnson counter 10

b. List and explain CMOS characteristics. 10

10a. Explain 2 input NAND gate TTL with a neat diagram. 6

b. Mention advantages and disadvantages of CMOS logic over TTL. 6

c. Give the VHDL code for the following :

i) Mod - 8 up counter ii) 2:4 priority encode. 8

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