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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. -Computer Science and Engineering

Semester End Examination, Dec - 2015

Digital Logic Design

Time: 3 hrs *Max. Marks: 100*

Note**: Answer any **FIVE** full questions, selecting **ONE** full question from each **unit.

UNIT - I

1 a. Simplify the following Boolean expression using Boolean Algebra, and implement the logic using NOR gates only — 6

$(x + xy)(\bar{x} + y) + yz$

b. Simplify the following expressions using K-map.

i) $F(w, x, y, z) = \Sigma m(0,1,3,7,8,12) + d(4,5,10,13,14)$ — 8

ii) $F(A, B, C, D) = \Pi m(2,3,10,11,12,13,14,15) + dc(0,1,6,7)$

c. Prove that A + AB = A. Find dual of the relation and also prove it using duality Theorem. — 6

2 a. Find prime implicants of the Boolean expression using Quine-McClusky method also find essential prime implicants — 12

$F(A, B, C, D) = \Sigma m(1,3,4,5,7,8,11,15)$

b. Using VEM method simplify the following

$F(A, B, C, D) = \Sigma m(0,4,8,11,12,14)$ — 8

i) Use 'A' as map entered variable

ii) Use 'D' as map entered variable.

UNIT - II

3 a. Design full adder and full subtractor using 4 x 1 multiplexer. — 8

b. Write a note on Read only memory. — 5

c. Implement the following functions using PLA

$F_1(A,B.C) = \Sigma m(0,2,7)$ — 7

$F_2(A,B.C) = \Sigma m(1,3,6)$

4 a. Explain 1 bit magnitude comparator circuit with example. — 10

b. Explain the design of 2-bit Fast adder. — 10

Contd……2

UNIT - III

5 a. Derive characteristic equations for
   (i) SR Flip Flop
   (ii) D Flip flop
   (iii) JK Flip Flop
   (iv) T Flip flop — 8

b. What is the difference between pulse triggered flip-flop and edge triggered flip flop. — 2

c. Explain the Design of JK master slave Flip flop. — 10

6 a. Design the following counters using Shift register
   (i) Johnson counter
   (ii) Ring counter — 12

b. Explain the design of serial in parallel out shift register. — 8

UNIT - IV

7 a. Design mod-6 synchronous counter using T flip-flop. — 10

b. Design self correcting mod 7 synchronous counter using D flip-flops (All unused status must lead to state 0). — 10

8 a. Explain the design of 4-bit D to A counter with a diagram. — 10

b. With a diagram explain the working of successive approximation ADC. — 10

UNIT - V

9 a. Write the VHDL code for the following:
   (i) 4 x 1 MUX
   (ii) 8 x 3 ENCODER
   (iii) FULL ADDER — 6

b. With suitable diagram explain the operation of 2 input TTL NAND gate with totempole output. — 10

c. Explain the working of CMOS inverter. — 4

10a. Explain the semiconductor switches used in Digital integrated circuits. — 12

b. Write VHDL code for the following :
   i) 3 x 8 Decoder
   ii) 'D' Flip Flop — 8

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