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P.E.S. College of Engineering, Mandya - 571 401
(An Autonomous Institution affiliated to VTU, Belgaum)
Third Semester, B.E. - Computer Science and Engineering
Semester End Examination; Dec - 2016/Jan - 2017
Logic Design

Time: 3 hrs   Max. Marks: 100

Note: Answer **FIVE** full questions, selecting **ONE** full question from each unit.

UNIT - I

1 a. Define Universal gates. Implement Basic gates using any one Universal gate. — 7

b. List and explain TTL characteristics. — 6

c. Simplify the following Boolean function using K-map and draw the equivalent logic circuit,

$f(A, B, C, D) = \Pi M(0, 1, 2, 3, 4, 6, 10, 11, 13)$. — 7

2 a. Describe CMOS characteristics. — 6

b. Get the simplified expression of,

$Y = F(P, Q, R, S) = \Sigma m(0, 4, 8, 10, 11, 12, 14, 15)$ using Quine Mc-Clusky method. — 6

c. Design BCD to excess-3 code converter. — 8

UNIT - II

3 a. Design Full adder and Full subtractor using suitable multiplexer. — 10

b. Design 2 bit Fast adder and justify you design. — 6

c. Write a VHDL code for 1 bit magnitude comparator. — 4

4 a. Design programmable logic array for the following Boolean functions:

$F_1(A, B, C) = \Sigma m(0, 3, 5, 7)$

$F_2(A, B, C) = \Sigma m(0, 4, 6, 7)$

$F_3(A, B, C) = \Sigma m(0, 4, 6)$. — 6

b. Explain the working of 8 bit binary adder subtractor circuit. — 8

c. Implement the following Boolean function using 8:1 MUX,

$F(W, X, Y, Z) = \Sigma m(0, 3, 4, 6, 10, 14, 15) + d(2, 5, 8, 11)$. — 6

UNIT - III

5 a. Differentiate between positive edge triggered and negative edge triggered clock pulses. — 4

b. Convert JK Flip-Flop to SR Flip-Flop. — 8

c. List the types of registers and explain with neat logic diagram. — 8

6 a. Describe Master-Slave JK Flip-Flop. — 8

b. Convert D Flip-Flop to SR Flip-Flop. — 8

c. List the Applications of shift registers and explain any two. — 4

UNIT - IV

7 a. Design 2 bit synchronous down counter using JK Flip-Flop.   6

  b. Design a sequential circuit using Moore model for a given sequential input of '011'.   12

  c. Differentiate between synchronous counter and asynchronous counter.   2

8 a. State the rules for state assignment.   10

  b. Design synchronous Mod-5 counter using clocked JK Flip-Flop.   10

UNIT - V

9 a. Explain D/A accuracy and resolution.   6

  b. Describe single Ramp-A/D converter.   10

  c. Find the binary equivalent weight of each bit in a 4 bit system.   4

10 a. Explain successive approximation weight of each bit in a 4 bit system.   10

  b. Explain 2 bit simultaneous A/D converter.   10

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