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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Sixth Semester, B.E. - Computer Science and Engineering

Semester End Examination; June - 2016

Advanced Computer Architecture

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain the elements of modern computers with neat diagram. 10

b. Explain vector supercomputers architectures. 5

c. Explain the operational model of an SIMD computer. 5

2 a. Briefly explain different types of data dependencies and hence draw the dependence graph for the following code segment,

S1 : Load R_1, A

S2 : Add R_2, R_1

S3 : MOV R_1, R_3

S4 : Store B, R_1 10

b. Explain different program flow mechanism and hence compare the same. 10

UNIT - II

3 a. Explain the pipelined execution of successive instructions in a base scalar processes. 5

b. List and explain any five differences between CISC and RISC architectures. 5

c. Explain typical VLIW processor architecture and its format. 10

4 a. With the neat diagram explain the addressing and timing protocols. 8

b. Explain different types of bus arbitration methods with neat diagrams. 6

c. With a neat block diagram explain two types of inter leaned memory organizations. 6

UNIT - III

5 a. Consider the following non-linear pipeline reservation table and find the following :

		Time							
		1	2	3	4	5	6	7	8
Stages	S_1	X					X		X
	S_2		X		X				
	S_3			X		X		X	

10

i) What are the forbidden latencies? ii) Draw state transition diagram.

iii) List all the simple cycles and greedy cycles.

iv) Determine the constant latency cycles and minimum average latency.

v) Let the pipeline clock period be t = 20 ns. Find the throughput of this pipeline.

Contd… 2

b. With respect to the mechanisms, for instruction pipe lining, explain internal data forwarding and Hazard avoidance mechanisms. 10

6 a. Consider the execution of a program of 15,00,000 instructions by a linear pipeline processor with a clock rate of 1000 MHz. Assume that the instruction pipeline has 5 stages and that one instruction is issued per clock cycle,

i) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non pipelined processor with an equal amount of flow through delay. 4

ii) What are the efficiency and throughput of this pipelined processor?

b. Briefly explain the methods of static and dynamic branch handling strategies. 6

c. Explain arithmetic pipeline design and draw a pipeline unit for fixed-point multiplication of 8-bit integers. 10

UNIT - IV

7 a. What is Cache coherence problem? Explain factors causing cache inconsistencies. 10

b. Explain cross bar switch and multiport memory with appropriate diagrams. 10

8 a. Explain different types of directory protocols with neat diagrams. 10

b. With neat diagram explain store forward and wormhole routing scheme of message passing. 10

UNIT - V

9 a. Explain the steps involved in developing parallel applications. 10

b. With block diagram explain shared address space protocol in scaling process. 10

10 a. What is scalability and explain different types of scalability? 10

b. Explain synchronous and asynchronous message passing protocols with neat diagrams. 10

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