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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Electrical and Electronics Engineering

Semester End Examination; Dec. – 2015

Digital Electronics

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer **FIVE** full questions selecting **ONE** full question from each **unit**.*
ii) Assume suitable missing data if any.

UNIT - I

1 a. Mention the advantages of digital systems over analog systems. 5

b. Construct the truth table for each of the following Boolean functions 10

i) $f(x,y,z) = yz + (\overline{x} + y)(\overline{x} + \overline{z})$ ii) $f(w,x,y,z) = wxy + \overline{w}(\overline{y} + z)$

c. Complement the following Boolean expressions, 5

i) $y = \overline{a}\overline{b}(ab + b\overline{d})$ ii) $y = \overline{a}\overline{b}(ab)$

2 a. State and prove Redundant Literal Rule (RLR) using relevant truth table. 6

b. Show that $y = f(A,B,C) = \sum(0,1,3,4,6,7)$ is the complement of $y = f(A,B,C) = \pi(2,5)$ 8

c. Draw the simplest possible logic diagram that implements the output of the logic diagram shown below 6

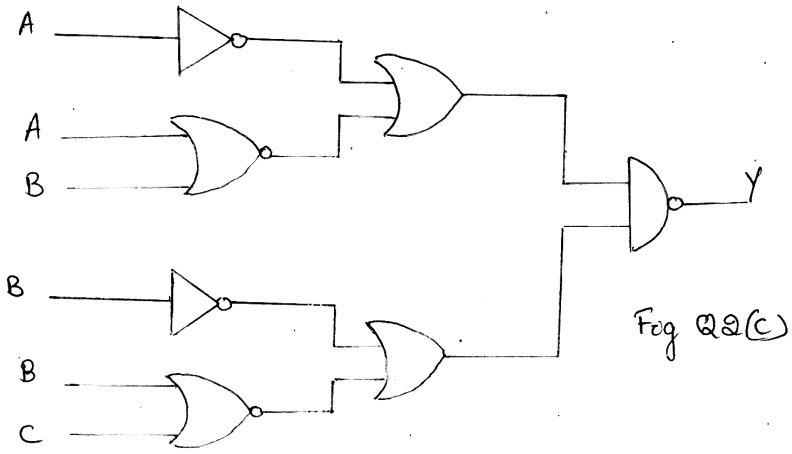

Fig Q2(c)

UNIT - II

3 a. Minimize and implement the following multiple output. Functions in SOP form using K-Map 10

i) $F = \sum m(1, 2, 5, 6, 8, 9, 10)$ ii) $F = \sum m(0, 1, 4, 6, 8, 9, 11) + d(2, 7, 13)$

b. Find a minimal sum for the Boolean function using Quine McClusky method and PI table reduction $F(a,b,c,d,e) = \sum m(0, 1, 9, 15, 24, 29, 30) + d(8, 11, 31)$ 10

4 a. Realize full subractor using only NOR gates. 8

b. Design a 4 – bit carry look ahead adder and write the logic circuit. 8

c. Draw the circuit of full adder using two half adders. 4

Contd…2

UNIT - III

5 a. Define encoder. Explain Decimal to BCD encoder with logic symbol, truth table and circuit diagram. 7

b. Implement the following function using a decoder minimizing the number of inputs to be summed, 5

$f_1(a,b,c) = \sum m(0,2,3,5,6,7)$ $f_2(a,b,c) = \sum m(1,3,4,6,7)$

c. Define demultiplexer and design 1:8 line DE – MUX with an illustrative truth table and circuit involving basic gates. 8

6. a. With the help of logic diagram and truth table explain DF/F and S. R F/F. 8

b. Distinguish between combinational and sequential circuits. 4

c. Explain the working of Master slave JK flip flop with logic diagram. 8

UNIT - IV

7 a. Explain Mealy and Moore Models of a clocked sequential circuit. 10

b. Design a 3 – bit synchronous up counter using JK flip – flops. 10

8 a. With a neat logic diagram, explain the working of a 4 – bit PISO register. 10

b. Distinguish between synchronous and asynchronous counter. 4

c. Explain the operation of 4 – bit Johnson counter with the help of logic diagram and state diagram. 6

UNIT - V

9 a. Explain the operation of 4 – bit binary weighted DAC and also derive the expression for a output voltage. 10

b. Determine the output voltage of the circuit as shown in Fig. Q. (b) when digital inputs are 0010 and 1010. 5

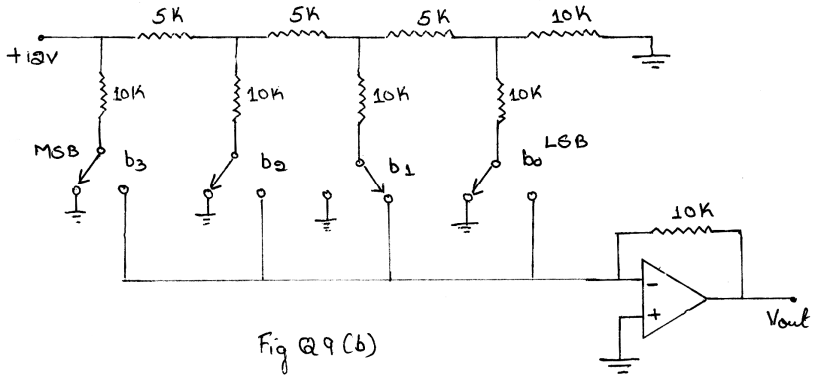

Fig Q9 (b)

c. Explain the operation of flash ADC. 5

10 a Define the following terms: 8

i) Fan out ii) Noise Margins iii) Propagation delay iv) Power dissipations

b. Explain briefly Emitter Coupled Logic (ECL) with circuit diagram. 6

c. Draw and explain MOS inverter circuits. 6

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